**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Patent Application of:

Hiroji Kawai

Application No.: 09/768,912

Confirmation No.: 5026

Filed: January 24, 2001

Group Art Unit: 2828

Examiner: James A. Menefee



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For: NITRIDE III-V COMPOUND SEMICONDUCTOR DEVICE (As Amended)

11/26/02

**AMENDMENT UNDER 37 C.F.R. § 1.111**

Commissioner Of Patents and Trademarks
Washington, D.C. 20231

Sir:

In response to the Non-Final Office Action dated July 18, 2002, Paper No. 11, please amend the above-identified application as follows:

**IN THE SPECIFICATION:**

**Page 3, please replace the first full paragraph continuing to page 4, with the following new paragraph:**

For thinning a GaAs substrate, primary lapping using a granular abrasive material of SiC or alumina is first conducted. Then, by using abrasive grains of a grain size of 1 μm or less of $CeO_2$, $ZrO_2$, $CrO_2$, or the like, the substrate is polished on a soft polisher such as synthetic resin or artificial leather to remove processing strain by lapping. As a result, the remainder depth of the processing strain is reduced to 10 μm or less, but additional processing by wet etching may be applied. As to the via hole to be made in the GaAs substrate, since GaAs is readily dissolved by any of sulfuric acid/hyrdogen peroxide solution or alkali solution, wet etching using such solution as the etchant is essentially sufficient for making the via hole. However, since side etching becomes large with wet etching and it is difficult to control the shape of the via hole, reactive ion etching (RIE) or ion milling is used normally. When using RIE for making the via hole, an etching rate as high as 50 to 100 μm/hr can be obtained, and the via hole can be made easily, by using a mixed gas of $CCl_2F_2$ and He as the etching gas and using a silicon oxide ($SiO_2$)